



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER OF PATENTS AND TRADEMARKS  
Washington, D.C. 20231  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/941,963	08/28/2001	Sunfei Fang	01P14755 US	7736

25962 7590 08/28/2002  
SLATER & MATSIL, L.L.P.  
17950 PRESTON RD, SUITE 1000  
DALLAS, TX 75252-5793

EXAMINER  
LEE, HSIEN MING

ART UNIT	PAPER NUMBER
2823	H

DATE MAILED: 08/28/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)
	09/941,963	FANG, SUNFEI
	Examiner Hsien-Ming Lee	Art Unit 2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on \_\_\_\_\_.

2a) This action is **FINAL**.                    2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 1-23 is/are pending in the application.

4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5) Claim(s) \_\_\_\_\_ is/are allowed.

6) Claim(s) 1-23 is/are rejected.

7) Claim(s) \_\_\_\_\_ is/are objected to.

8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) The proposed drawing correction filed on \_\_\_\_\_ is: a) approved b) disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) The oath or declaration is objected to by the Examiner.

#### Priority under 35 U.S.C. §§ 119 and 120

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some \* c) None of:

1. Certified copies of the priority documents have been received.

2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.

3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) The translation of the foreign language provisional application has been received.

15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

#### Attachment(s)

1) Notice of References Cited (PTO-892)

2) Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2, 3.

4) Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_

5) Notice of Informal Patent Application (PTO-152)

6) Other: \_\_\_\_\_

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

- (e) the invention was described in–
  - (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
  - (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

2. Claims 1-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Nakagawa et al. (US 2001/0049150 A1).

Regarding claims 1-8, 10-15, Nakagawa et al. identically teach the claimed method of cleaning a hole as shown in Fig. 10B in an organic inter-level dielectric (ILD) 2, the hole having sidewalls and a bottom, the organic ILD disposed on a semiconductor substrate 1, the method comprising: (1) performing a radio frequency (RF) sputter clean of the hole, i.e. utilizing the RF etching system as shown in Fig. 7, wherein a RF generator 23 is used (refers to section [0226]), to clean or etch an **oxide layer 32** on the bottom of the hole using **Ar** or **He** 31 as cleaning gas (refers to sections [0265] and [0270]), wherein the Ar cleaning acts as a **physical** etch approach; and (2) performing an anisotropic, ion enhanced organic etch of the hole at least partially during the sputter clean, i.e. utilizing a cleaning gas including CH<sub>3</sub>NH<sub>2</sub> (sections [0262]~[0264]) or carbon, hydrogen and nitrogen (section [0273]) to **anisotropically etch** the organic ILD 2 to form the hole, wherein the organic etch acts as a **chemical** etch approach. The RF sputter clean and the organic etch are performed at the same time by the same plasma since the clean step and

Art Unit: 2823

the etch step are performed over about the same time interval simultaneously using the mixed gas of CH<sub>3</sub>NH<sub>2</sub> and Ar ( refers to section [0263]).

Regarding claim 9, Nakagawa et al. also teach that the hole is part of an interconnect structure, wherein a conductive layer at a bottom of hole as shown in Fig. 12A, wherein a composite conductive layer 112/113/114 is at the bottom of the hole 118; and the ILD dielectric layer 115 is an organic film; and the sputter clean would remove a surface oxide formed on the bottom of the hole 118 over the conductive layer 112/113/114, just as the oxide layer 32 formed at the bottom of the hole as shown in Fig. 10B.

Regarding claims 16-21, Nakagawa et al., in another embodiment, also teach the claimed method of forming an interconnect through an organic ILD, the method comprising:

- forming a lower conductive layer 113 on a semiconductor substrate 111 (Fig.11A);
- forming the organic ILD 115 on the lower conductive layer 111 (Fig.11A);
- etching a hole 118 through the organic ILD 115 down to the lower conductive layer 111 (Fig.12A);
- performing an RF sputter clean of a bottom of the hole;
- performing an anisotropic, ion enhanced chemical organic etch of the hole, as the same manner as mentioned above ( refers to section [0284]), wherein the etch is performed at least partially during the RF sputter clean;
- forming a plug 123 in the hole 118 (Fig.12D); and
- forming an upper conductive layer on the organic ILD and the plug ( refers to section [0286]), wherein the section [0286] states that after forming the plug the

Art Unit: 2823

aforementioned procedures are repeated as to form a connection plug and an interconnect, resulting in fabricating a multi-level interconnect structure.

Regarding claim 22, Nakagawa et al. also teach forming a lower cap layer 114, which can be silicon nitride ( section [0290]), on the lower conductive layer 113 before the forming of the organic ILD layer 115, and forming an upper cap layer 116 on the organic ILD layer 115 (Fig. 11b).

Regarding claim 23, Nakagawa et al. also teach forming a liner 119 in the hole 118 before forming the plug 123 (Figs. 12B-12D).

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsien-Ming Lee whose telephone number is 703-305-7341. The examiner can normally be reached on M-F (9:00 ~ 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 703-308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are 703-305-0142 for regular communications and 703-305-0142 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

*Lee*  
Hsien Ming Lee  
August 23, 2002

*Wael Fahmy*  
SUPERVISORY PRIMARY EXAMINER  
TECHNOLOGY CENTER 2800